SystemC-AMS

SystemC-AMS is a modeling library, developed by the Open SystemC Initiative AMS working group, allowing designers to simulate systems that combine data-flow modeling, analogue circuits and rather control oriented digital circuits. In ANDRES, SystemC-AMS is used for specification and modeling of analog/mixed-signal components. Additionally it is extended for explicit expression of adaptivity within system models.
To support fast and easy system level design of adaptive communication systems, a library of typical building blocks, focusing on the field of radio frequency systems, is being developed.

HetSC

HetSC is a methodology enabling heterogeneous specification of complex embedded systems in SystemC. HetSC supports multiple formal Models of Computation, including untimed MoCs, synchronous MoCs and the timed MoCs already supported by SystemC. In ANDRES, HetSC will be used for modelling of embedded software

Partners

OFFIS, TU Vienna, KTH Vetenskap och Konst, UC Universidad de Cantabria, DS2, Thales

ANDRES

ANalysis and Design of run-time REconfigurable heterogeneous Systems

Most embedded systems are heterogeneous in nature, including components from different domains like digital hardware, analog hardware and software, each with its own design methods and tools. Additionally, run-time reconfigurable architectures are becoming more attractive but are rarely supported by any design methodologies. Adding this to the ever growing complexity of embedded systems, there is a need for an integrating and seamless design flow explicitly supporting the integration of adaptive applications and architectures.

The ANDRES project is developing a new design methodology based on the modeling language SystemC for modeling, simulation and synthesis of adaptive heterogeneous embedded systems. It is a specific targeted research project (STREP) within the Sixth Framework Programme (FP6) of the EU.

Project Facts

Funding	EC, IST-5-033511
Type	STREP
Duration	June 2006 – May 2009
Volume	31 person years
Website	http://andres.offis.de

Motivation

Today's embedded systems are usually composed by components from different domains such as digital hardware, analog hardware and software. Each of these domains comes with its own methods and tools for design and implementation, shifting system integration and validation to the very end of the design process. In addition, the growing demand for greater flexibility and reduced time-to-market can only be met by using new run-time reconfigurable platforms, like dynamically reconfigurable FPGAs or switched-capacitors. However, such adaptive applications and architectures are not supported by current high-level design methodologies. So adding heterogeneity and adaptivity to the ever growing complexity of embedded systems, the already costly design process is getting even more time-consuming and error-prone.

Project Goals

Primary goal of the ANDRES project is the development of a SystemC based design flow considering heterogeneity and adaptivity as two important aspects of embedded application design. Integral part of the methodology is a modeling framework including three domain specific modeling libraries and flexible communication interfaces for easy integration of components into an overall system. Such system models can be simulated and analyzed using one common simulation environment.
The design flow is completed by methods and tools for automatic synthesis and implementation of high-level adaptive application models to dynamically reconfigurable hardware.
The ANDRES methodology is evaluated by state-of-the-art industrial use cases from the fields of software-defined-radio and powerline communications.

OSSS+R

OSSS+R is an approach to use object-oriented features to model reconfigurable digital hardware systems in SystemC. In OSSS+R, adaptivity is an integral part of the application rather than a just technical aspect of the underlying platform. By hiding the technical details of how the adaptation is implemented, OSSS+R allows designers to concentrate on the application design. Being based on OSSS (Oldenburg System Synthesis Subset), it also enables transaction level modeling of cycle-accurate models using method-based communication. OSSS+R models can be simulated using the provided SystemC based simulation library.
Unlike other high-level design methodologies, OSSS+R has been designed with synthesis in mind. Therefore, as an extension of the synthesizable subset of SystemC, all modeling elements have well-defined synthesis semantics. The ANDRES project is developing tools to enable automatic synthesis and implementation of digital adaptive application models written in OSSS+R to dynamically reconfigurable hardware.